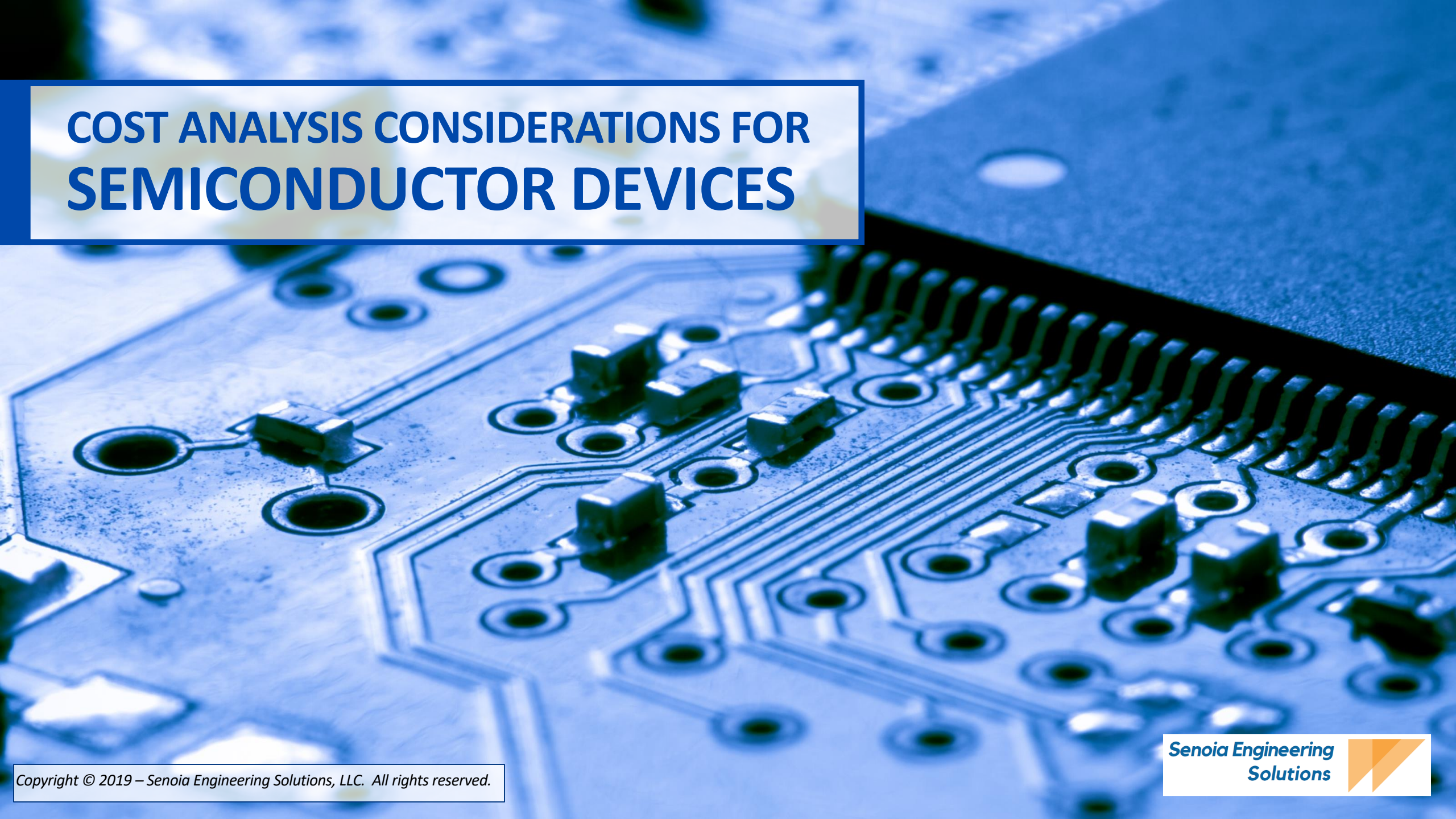
Senoia Engineering Solutions

COST ANALYSIS CONSIDERATIONS FOR SEMICONDUCTOR DEVICES



Senoia Engineering Solutions

INTRODUCTION

> **Jeff Miller**
President and Owner
Senoia Engineering Solutions, LLC

Education

- B.S. Electrical Engineering –
  Kettering University (Flint, MI)
- M.S. Industrial Engineering –
  Purdue University (West Lafayette, IN)
- MBA –
  Rollins College (Winter Park, FL)
- Certificate in Executive Management –
  University of Notre Dame (South Bend, IN)

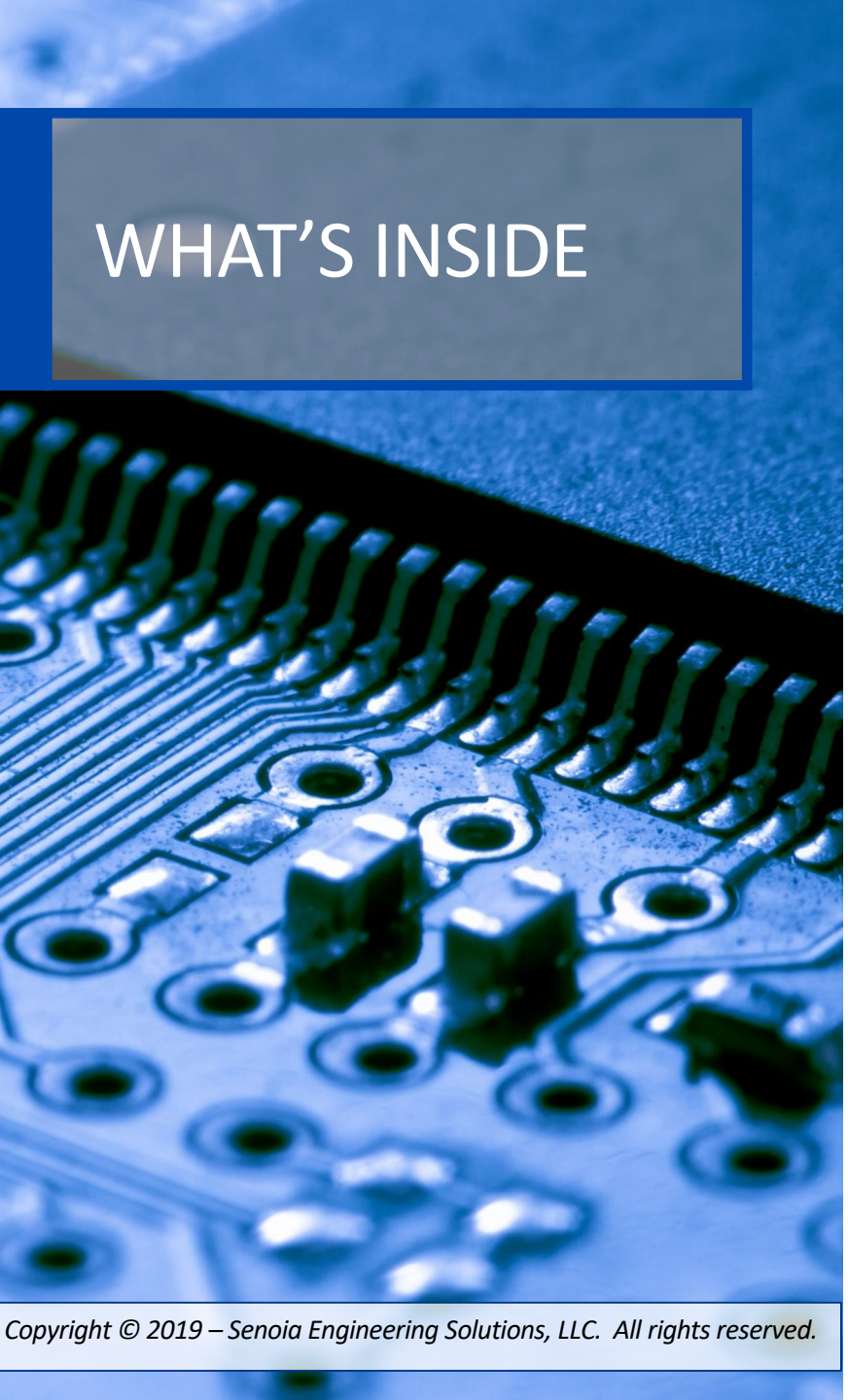
Experience

- 33 years of multifunctional experience within the electronics industry
  - *Automotive:* GM, Ford, Standard Motor Products, Panasonic
  - *Agriculture:* John Deere
  - *Major Appliance:* Whirlpool Corporation
- Over 11 years experience in cost engineering & VEVA of electronics and electrical assemblies

Other

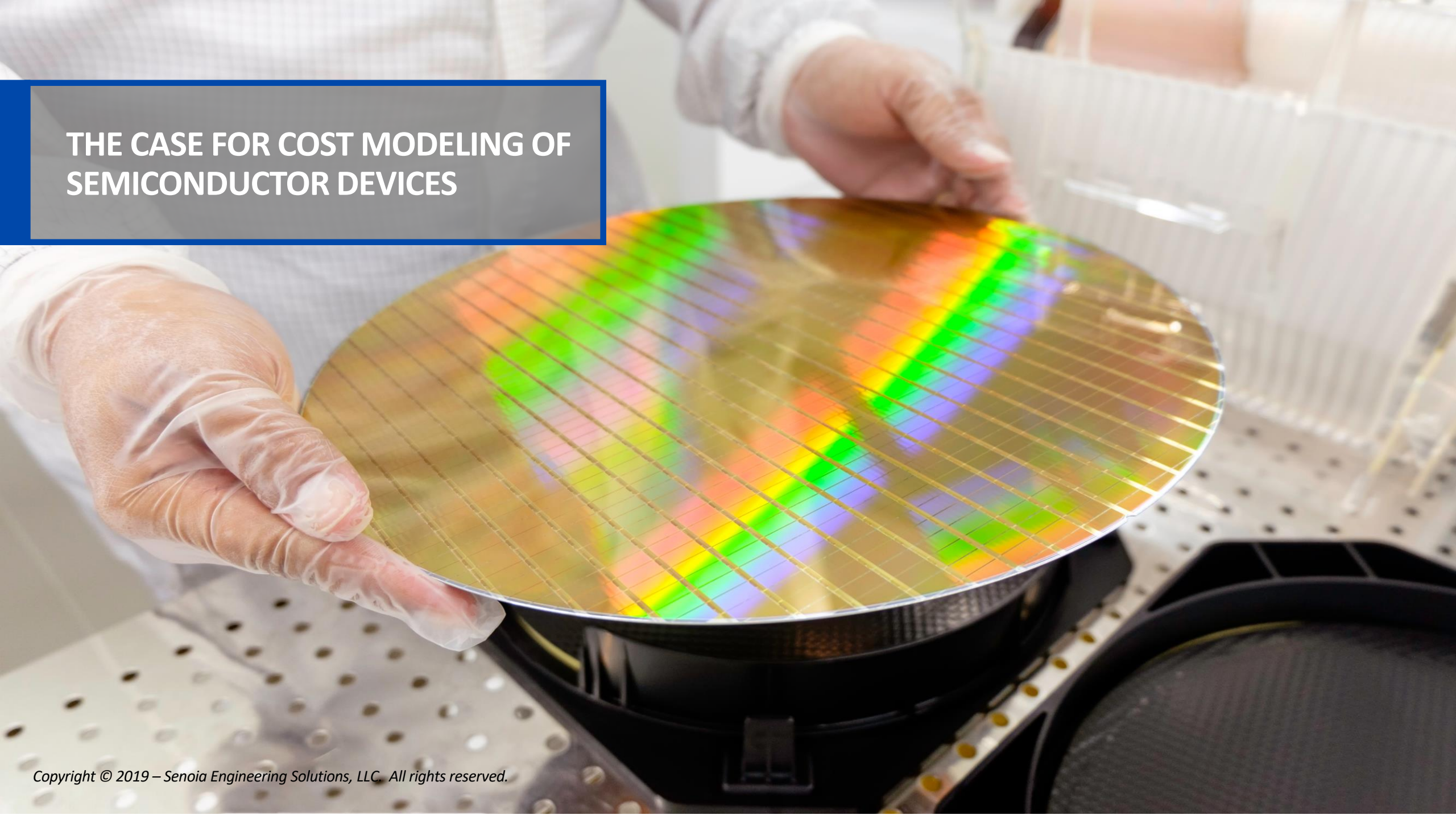
- Contributing author: "Realistic Cost Estimating for Manufacturing – 3rd Edition"

  Published by the Society of Manufacturing Engineers – edited by Michael Lembersky

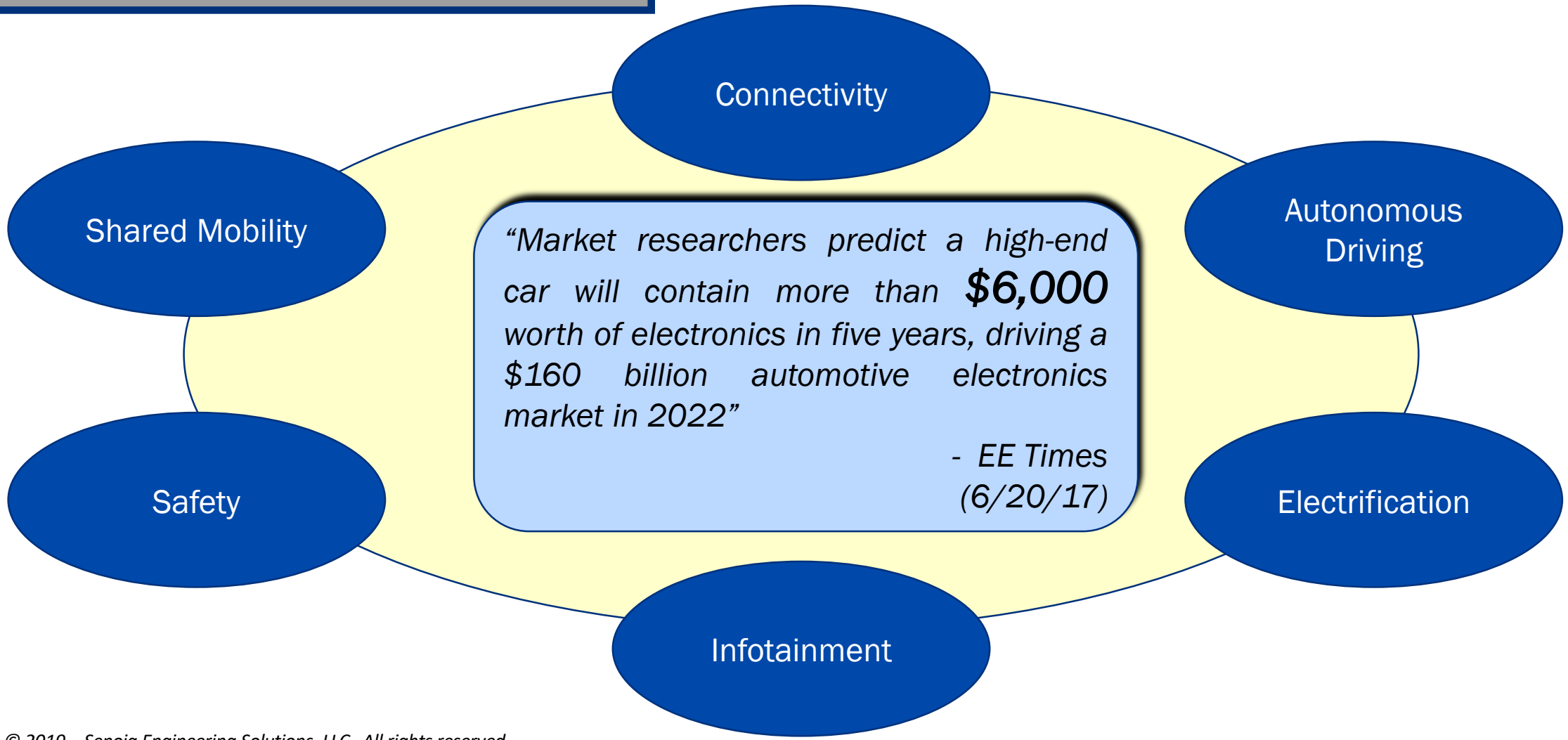


WHAT'S INSIDE

THE CASE FOR COST MODELING OF SEMICONDUCTOR DEVICES



INCREASING SILICON CONTENT OF FUTURE AUTOMOBILES



"Market researchers predict a high-end car will contain more than ***$6,000*** *worth of electronics in five years, driving a $160 billion automotive electronics market in 2022"*

- EE Times (6/20/17)

SEMICONDUCTOR DEVICES – FAMILY OVERVIEW

Microelectromechanical Systems (MEMS)

- Accelerometers
- Pressure Sensors
- Micro-machined sensors and actuators

Discrete Devices

- Diodes
- Transistors
- Insulated Gate Bipolar Trans. (IGBT)
- Field Effect Transistors (FET)
- Silicon Controlled Rectifiers (SCR)
- Thyristors

Monolithic Integrated Circuits (IC)

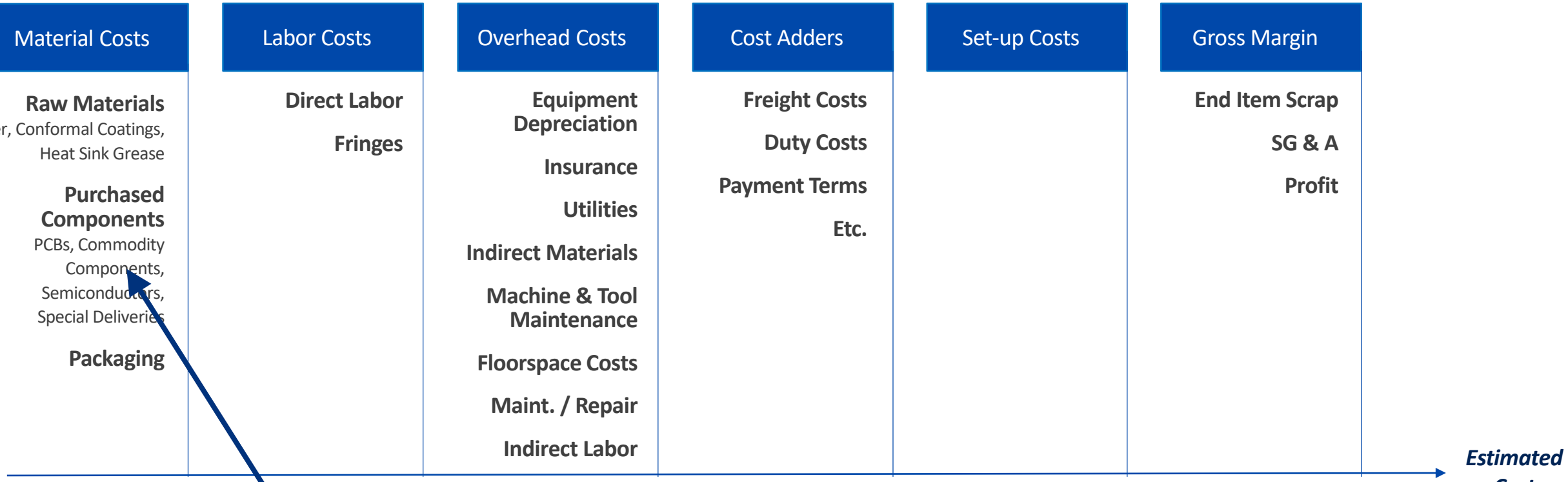
- Microprocessors
- Microcontrollers
- Memory Devices
- Analog / Linear ASICs

Optoelectronic Devices

- Laser Diodes
- Charge Coupled Devices (CCD)
- Light Emitting Diodes (LED)
- Solar Cells

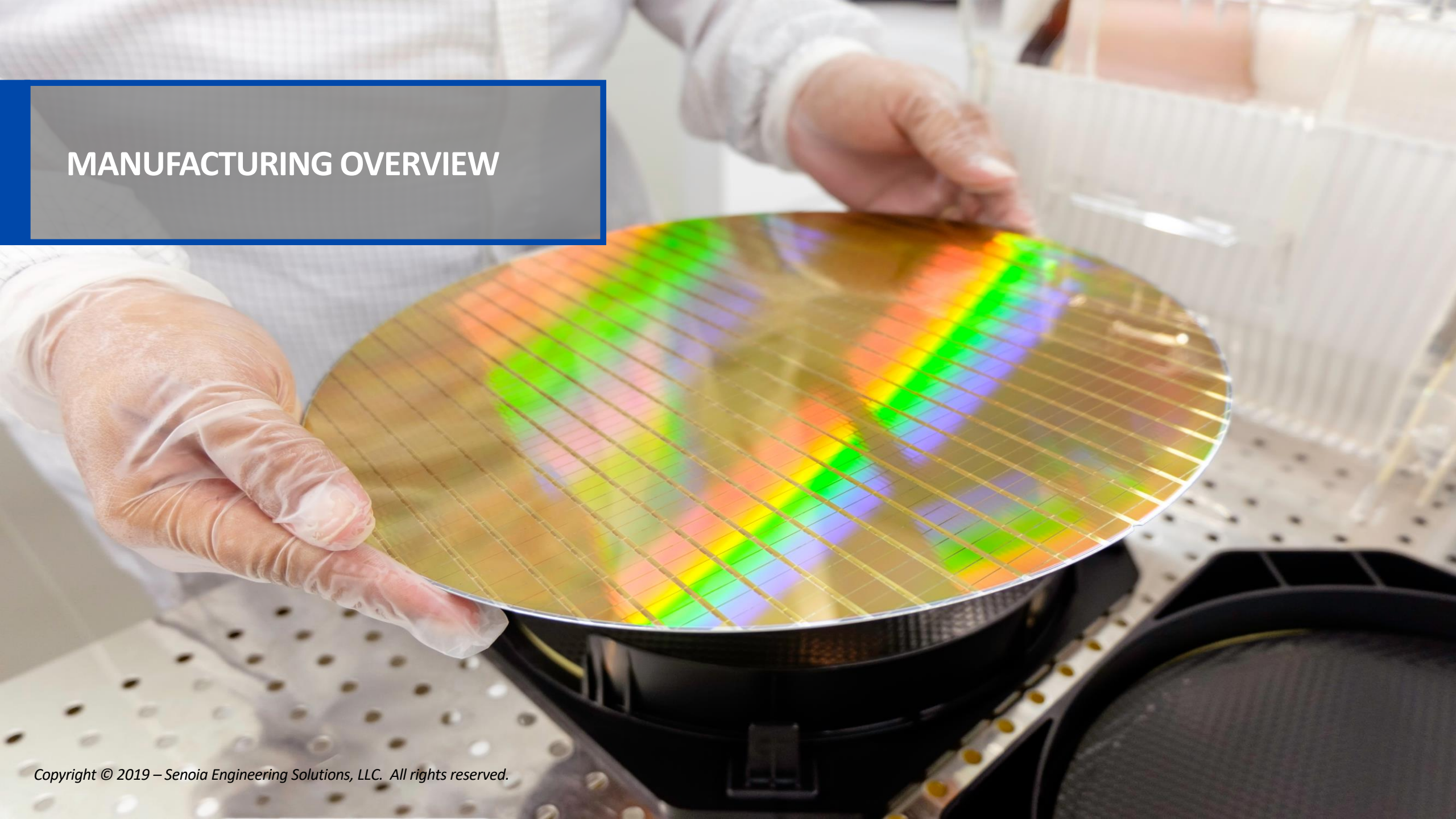
Self-driving vehicles will use ALL of these device families – and more !!

COST ELEMENTS – TYPICAL ELECTRONIC ASSEMBLY



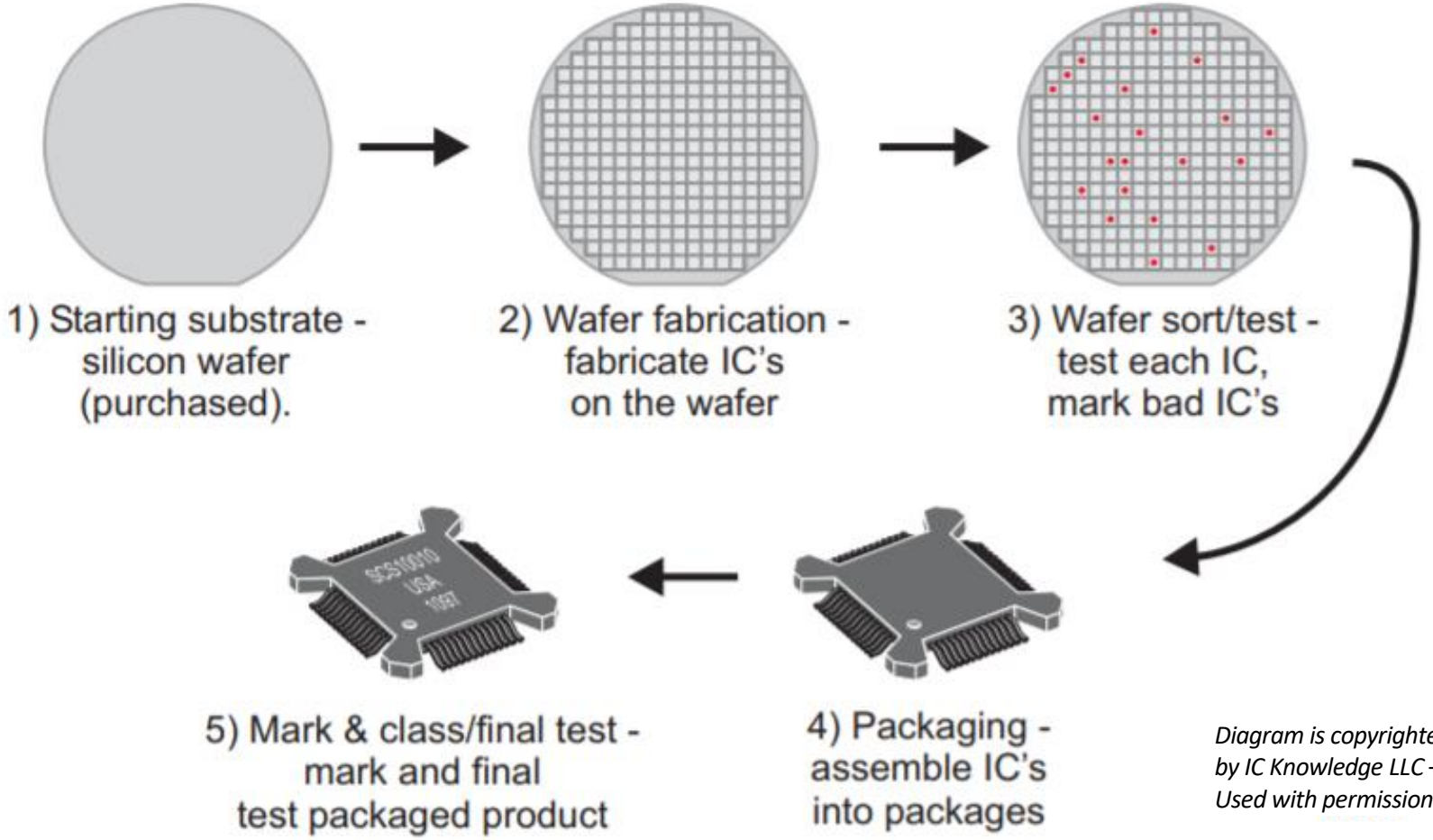
- **Majority of costs typically comes from purchased components**
- **Semiconductors can represent 50% - 80% of material costs**

MANUFACTURING OVERVIEW



SILICON WAFER MANUFACTURING PROCESS

Five Basic Process Steps:



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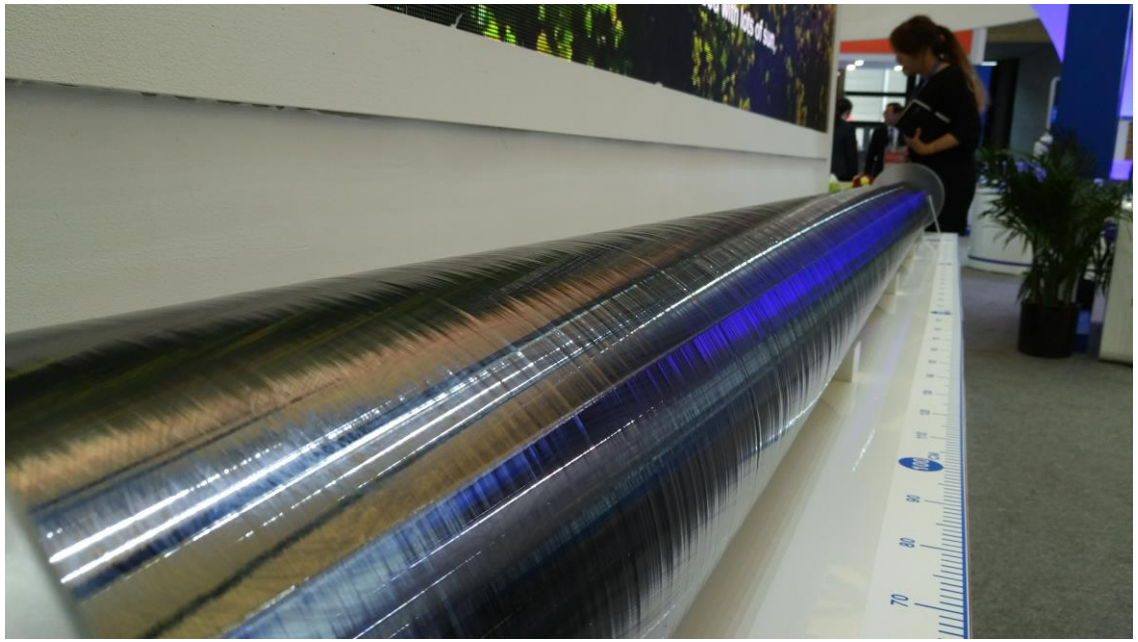
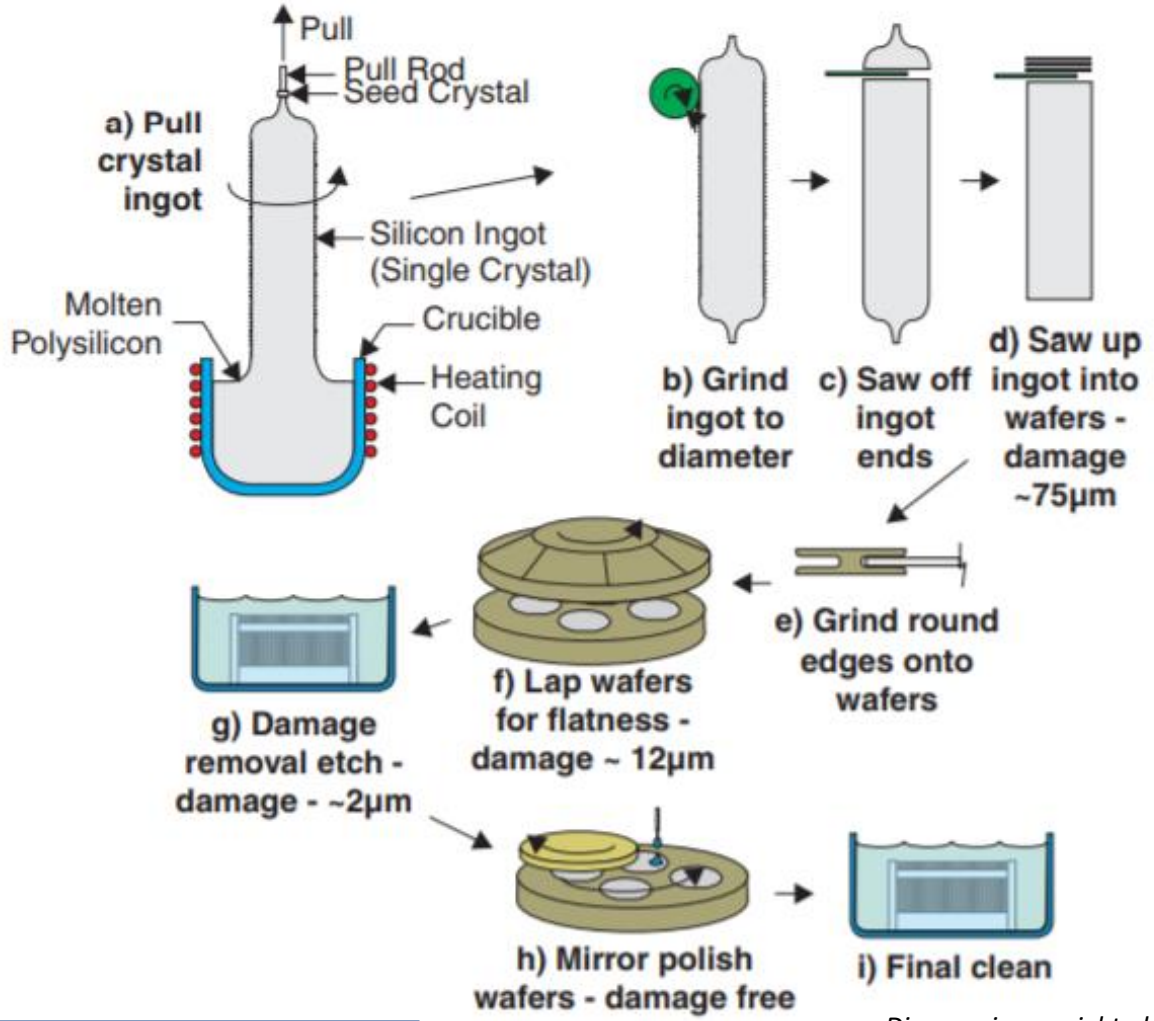
STEP 1: STARTING SUBSTRATE





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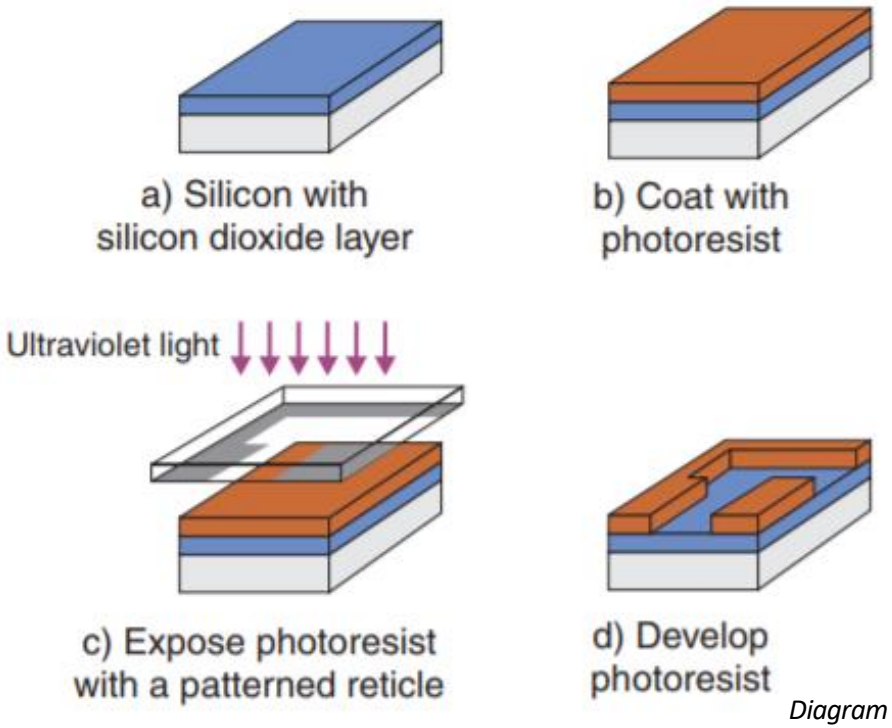
- Starting material is typically purchased from a Tier 2 supplier to the fab.
- Czochralski process is used to grow pure ingot with uniform crystal matrix.

STEP 2: WAFER FABRICATION

- Fabrication is performed in a clean room environment using photolithographic techniques.
  - Some companies utilize third party foundries (TSMC, SSMC, etc.)
- Steps are repeated multiple times to build circuit structures.
  - Resistors, transistors, conductors, etc.
  - Time to build circuit structures can range from 15 – 200 days.
- Final passivation layer protects the circuit from contamination and damage.



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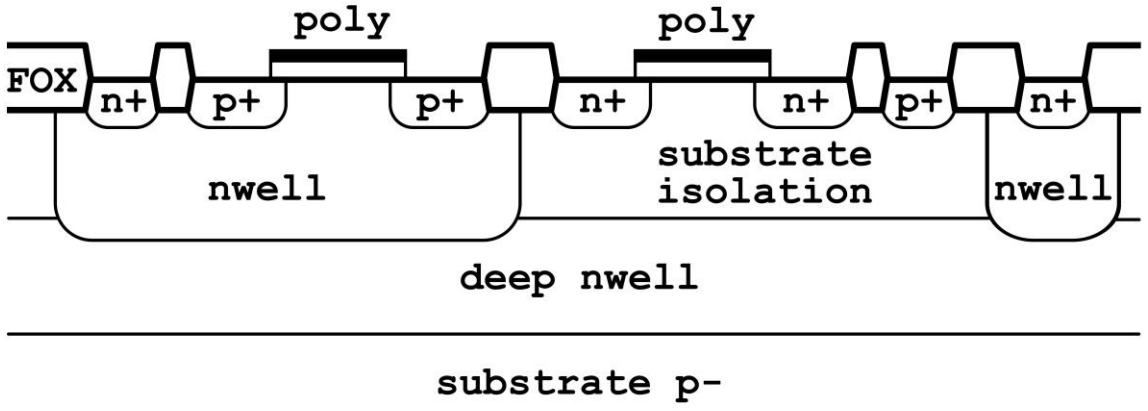


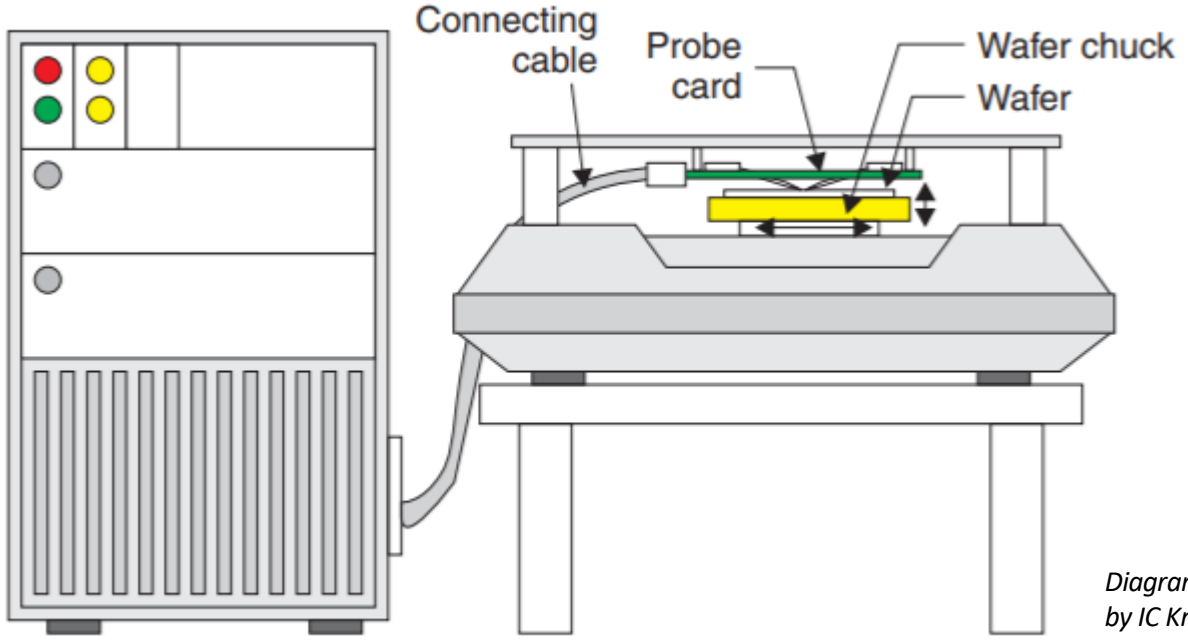
Cross-section: typical CMOS transistor structure

CLEAN ROOM FACILITIES

- Fabrication of microscopic geometries (typ. 20 nm) on the semiconductor device requires special clean rooms:
  - Class 1000: “1000 particles or less of contaminates per 1 cubic foot of air.”
  - For comparison: hospital surgery room is Class 10,000
- Operators wear “bunny suits” to limit human body particulates.
- Air flow is top-down and filtered.
- A single foreign particle in the wrong place can render a device to be useless.
  - CMOS geometries can be as small as 20 nm
  - In comparison:
    - Red blood cell is 6000 nm in length
    - Ebola virus is 1500 nm in length

STEP 3: WAFER TEST

- Each die is probed and run through a series of electrical tests to verify functionality and parametric characteristics.
- Bad die are marked with an ink dot, for separation at later operation.



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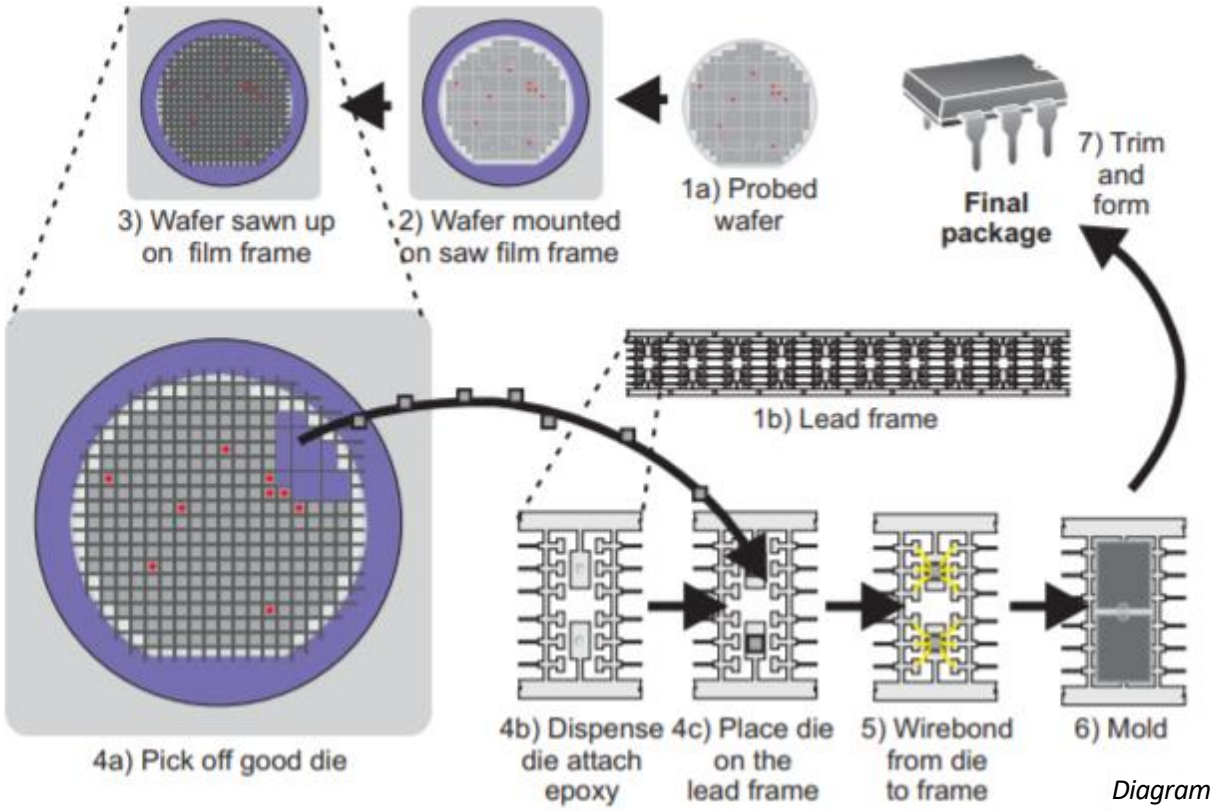
Key Take-Away:

- **"Commercial Grade" devices are tested at room temperature.**
- **"Automotive Grade" devices are tested at cold, room, and hot temperatures.**

STEP 4 and 5:
BACK-END PROCESSES



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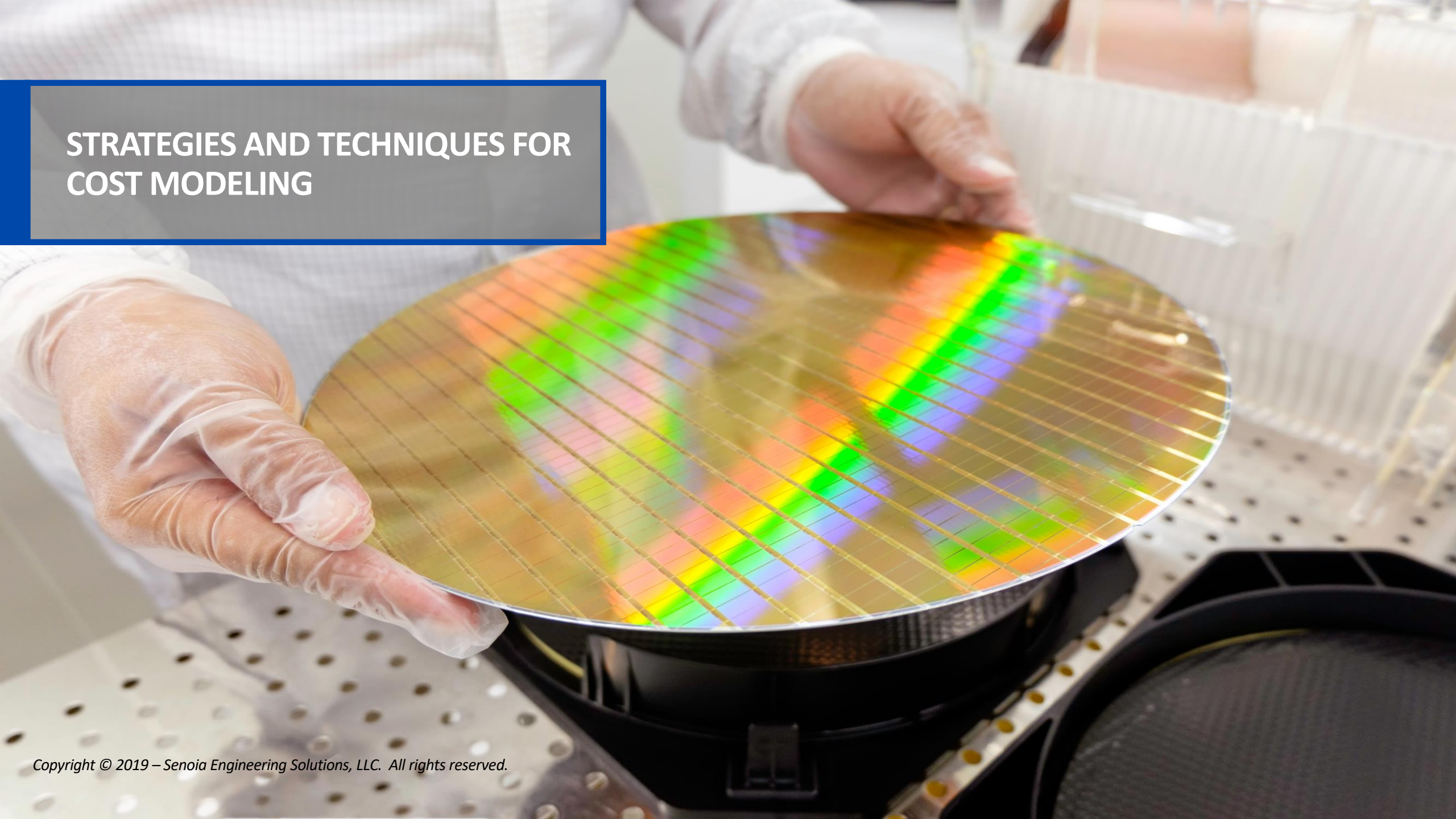
- Back-End Processes include:
  - Dicing Saw
  - Die Sort (Pick-And-Place)
  - Interconnect
  - Package Assembly
  - Final Electrical Test
  - Labeling
- Frequently performed by 3rd parties.

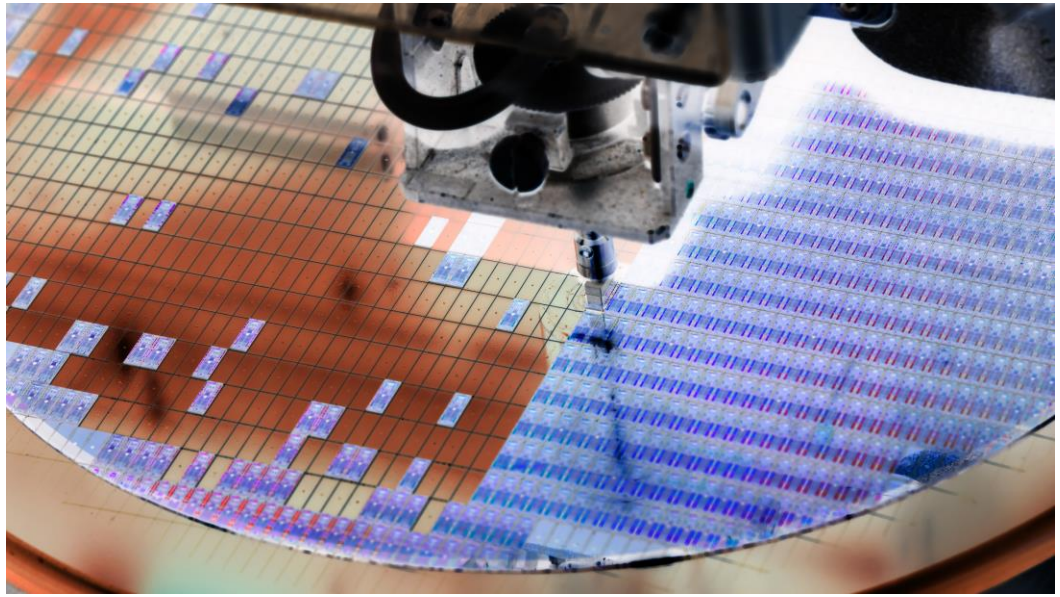
STRATEGIES AND TECHNIQUES FOR COST MODELING

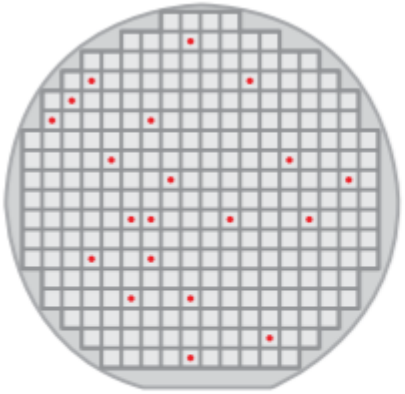


DIE SIZE vs WAFER YIELD

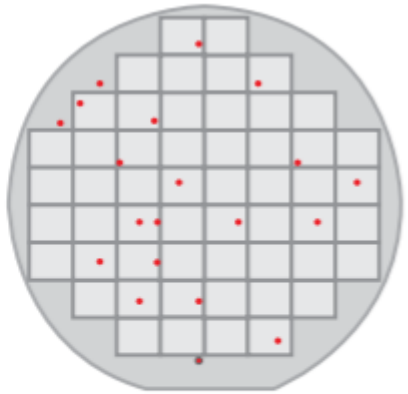
Die size is inversely correlated with wafer yield.

- Larger die will have lower yields.





20 Defects
20 Bad Die
264 Gross Die
92% Yield



20 Defects
16 Bad Die
54 Gross Die
70% Yield

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Larger die sizes typically have lower wafer yields.

PRODUCT LIFE CYCLE IMPACT TO SEMICONDUTORS

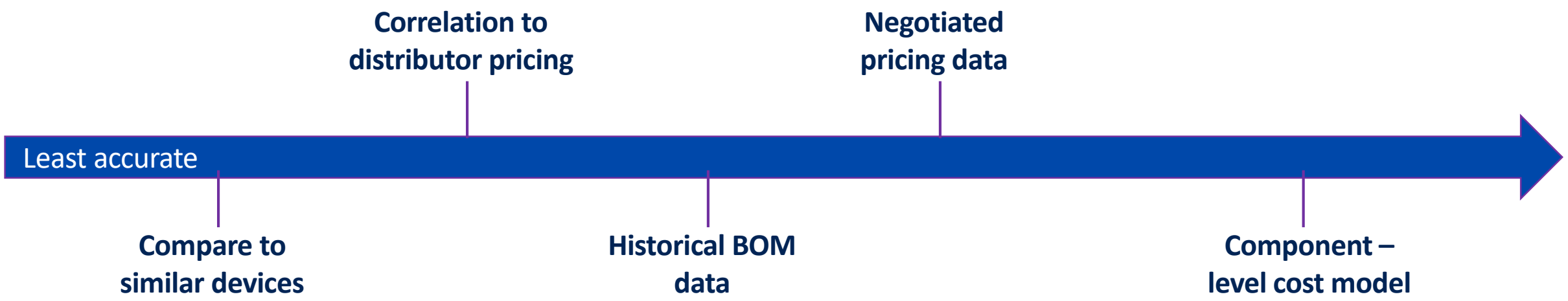
ANSI / EIA-724-97 Product Life Cycle Data Model:

	Stage 1: Intro	Stage 2: Growth	Stage 3: Maturity	Stage 4: Saturation	Stage 5: Decline	Stage 6: Phase Out
Price	Highest	Declining	Stable	Level	Increasing	Lifetime Buys
Customer Demand	Low	Increasing	Stable	Stable	Decreasing	High
# of Competitors	Few	High	Stable	Declining	Declining	Declining

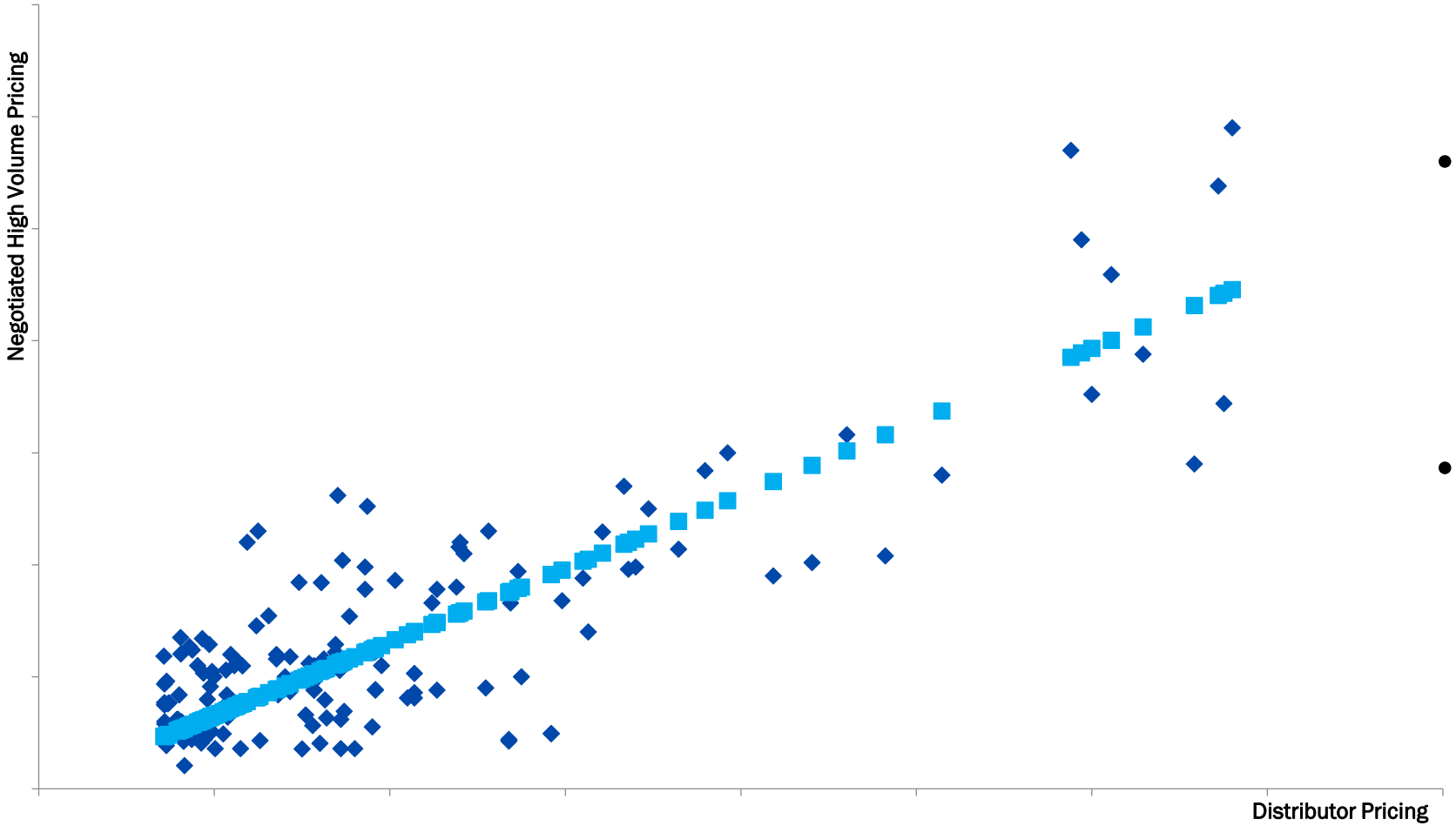
Life cycle stage will affect the cost of a given device.

STRATEGIES – COST ESTIMATING OF SEMICONDUCTORS

Multiple methods to estimate cost:



STRATEGIES – CORRELATION TO DISTRIBUTOR PRICING



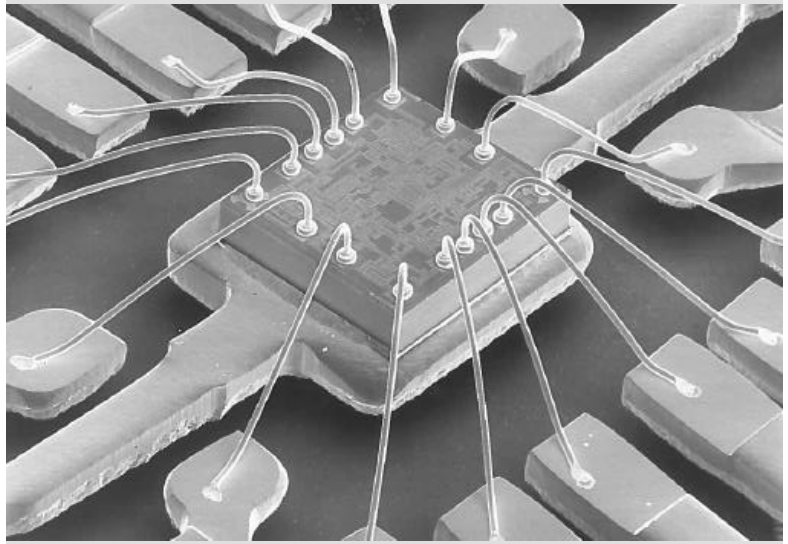
- Use regression techniques to correlate known high-volume device pricing to distributor pricing.
- General form of the linear equation:
  - $E(y) = b_1x + b_0 + e$

USE OF COMPONENT-LEVEL COST MODELS

- Use specialized cost models for estimating the semiconductor family under consideration.
- Examples:
  - IC Knowledge “Discrete and Power Device Cost and Price Model”
  - IC Knowledge “IC Cost and Price Model”
  - IC Knowledge “MEMS Cost and Price Model”
  - IC Knowledge “Assembly and Test Cost and Price Model”
- Access to material analysis equipment may be required: wet chemistry, SEM, x-ray, etc.
  - Key cost drivers reside at the die level.

Key IC Cost Drivers

- Production volume
- Fab process
  - Wafer size
  - Structure geometry
  - Process (i.e. CMOS, etc.)
  - # of mask layers (i.e. metal, poly, etc.)
- Die size
- Wafer Test Description
- Package
- Number of Pins



ACKNOWLEDGEMENTS

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President and Founder – IC Knowledge, LLC

www.icknowledge.com

Note: there is no commercial relationship between ICKnowledge, LLC and Senoia Engineering Solutions, LLC

Q & A

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